UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,128	09/16/2003	Ken Gary Pomaranski	200308565-1	4003

22879 7590 11/03/2005

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
KIM, DANIEL Y	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,128	POMARANSKI ET AL.	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, 6-16, 29-30 and 32-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Jeddeloh (US Patent No. 6,363,502).

For claim 1, Jeddeloh discloses a system, comprising:

a memory mapping logic configured to provide access to memory locations (memory remapping module maps defective memory addresses to non-defective memory addresses, col. 5, lines 54-57, abstract), where the memory mapping logic can be configured to direct a memory accessing operation intended for one memory location to another memory location (col. 5, lines 54-57); and

a memory quality assurance logic operably connected to the memory mapping logic (memory controller with a plurality of different error handling modules... an error detection module, an error correct module, and a memory remapping module, col. 2, lines 33-40, fig. 1, items 38-42), where the memory quality assurance logic is configured to:

control copying contents between a first memory location and a second memory location (the processor accesses a remapping table that maps each defective memory portion of the requested memory bank to a non-defective memory portion of the requested memory bank, col. 7, lines 46-49);

reconfigure the memory mapping logic so that memory accessing operations intended for the first memory location are directed to the second memory location (the processor determines the non-defective remapped location to which the defective requested memory portion was mapped, col. 7, lines 49-51); and

initiate memory testing of the first memory location (the processor then accesses the remapped memory portion and performs the requested operation on the remapped memory portion, col. 7, lines 52-54).

For claim 3, Jeddeloh discloses the memory mapping logic includes one or more address translation tables (a remapping table that maps each defective memory portion of the requested memory bank to a non-defective memory portion of the requested memory bank, col. 7, lines 46-49).

For claim 6, Jeddeloh discloses the memory quality assurance logic is configured to selectively logically replace the first memory location with the second memory location by reconfiguring the memory mapping logic, based, at least in part, on a result from the memory testing of the first memory location (col. 7, lines 40-60 and fig. 6, items 122-132).

Claim 7 is rejected using the same rationale as for the rejection of claim 6 above.

For claim 8, Jeddeloh discloses the memory quality assurance logic is configured to initiate memory testing of the first memory location by sending one or more signals to a memory testing logic (the memory controller processor employs the control lines to inform a selected one of the error detection and error correction modules whether the memory access request includes a read or a write request, col. 5, lines 15-18).

For claim 9, Jeddeloh discloses the memory quality assurance logic is configured to initiate memory testing of the first memory location by sending one or more signals to an onboard memory testing logic, where the onboard memory testing logic is physically connected to the first memory location (col. 5, lines 15-18 and fig. 3, items 38A and 12A).

For claim 10, Jeddeloh discloses the memory quality assurance logic selects the second memory location (accesses the remapped memory portion and performs the requested operation, col. 7, lines 52-54 and fig. 6).

For claim 11, Jeddeloh discloses the memory quality assurance logic includes one or more data stores configured to store one or more of, a memory freshness data, a memory quality data, an operating system instance to physical memory location relationship data, and a memory reconfiguration data (memory controller includes a configuration array with configuration registers that keep track of which of the plurality of error handling modules is employed for each of the memory banks, col. 3, lines 43-47).

Claim 12 is rejected using the same rationale as for the rejection of claim 11 above. Jeddeloh further discloses the memory quality assurance logic being operable connected to the one or more data stores (fig. 3, items 38A-46A).

For claim 13, Jeddeloh discloses the second memory location is located in internal memory of the memory mapping logic (fig. 3, items 12A and 13A-20A).

For claim 14, Jeddeloh discloses the second memory location is located in internal memory of the memory quality assurance logic. (fig. 3, items 12A and 13A-20A).

For claim 15, Jeddeloh discloses the second memory location is physically connected to the first memory location (memory module includes first through four memory banks; the memory module could have more or less than the four, col. 3, lines 13-19 and fig. 1, items 12-20).

Claim 16 is rejected using the same rationale as for the rejection of claim 10 above.

Claim 29 is rejected using the same rationale as for the rejection of claim 1. Jeddeloh further discloses:

a processor (fig. 1, item 24);

a memory operably connected to the processor, where the processor can access the memory (fig. 1, item 12, 26, 22 and 85);

a memory mapping logic configured to provide access to memory locations in the memory, where the memory mapping logic can be configured to direct a memory accessing operation intended for one memory location to another memory location (fig. 1 item 42).

For claim 30, Jeddeloh discloses the system is embedded in a computer (a method and computer system for storing data subject to memory errors, col. 2, lines 31-32).

For claim 32, Jeddeloh discloses the memory quality assurance logic includes one or more data stores configured to store one or more of, a memory freshness data, a memory quality data, an operating system instance to physical memory location relationship data, and a memory reconfiguration data (each configuration register stores an indication of the error handling module that will be employed to write data to and read data from the memory block associated with the configuration register, col. 2, lines 46-49).

For claim 33, Jeddeloh discloses the memory quality assurance logic is operably connected to one or more data stores configured to store one or more of, a memory freshness data, a memory quality data, an operating system instance to physical memory location relationship data, and a memory reconfiguration data (fig. 3, items 46A, 38A, 40A and 56A).

For claim 34, Jeddeloh discloses a memory location selection logic configured to select the first memory location and the second memory location (processor accesses the requested memory portion, fig. 6, item 132; the processor then accesses the remapped memory portion, fig. 6, item 128).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh (US Patent No. 6,363,502) and Frisch (US Patent No. 5,721,828).

For claim 2, Jeddeloh discloses the invention as per the rejection of claim 1 above. Jeddeloh does not, however, expressly disclose that the memory mapping logic includes a crossbar.

Frisch, however, discloses a multicomputer memory access architecture made up of a crossbar network to which are connected processing nodes and I/O interface nodes, which establish communication paths through the crossbar networks in response to routing signals, so that a local processor has direct access to remote memory, which is mapped into local address space (abstract).

Jeddeloh and Frisch are analogous art in that they are of the same field of endeavor, that is, a system for the management of memory. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include a crossbar in such a system because this would allow routing of signals in local registers so that a processor can access memory in remote processing nodes (abstract), as taught by Frisch.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh (US Patent No. 6,363,502) and Vivio et al (US Patent No. 5,867,642).

For claim 5, Jeddeloh discloses the invention as per the rejection of claim 1 above. Jeddeloh does not, however, expressly disclose the memory quality assurance logic is configured to selectively logically remove the first memory location from a first set of memory by reconfiguring the memory mapping logic, based, at least in part, on a result from the memory testing of the first memory location.

Vivio, however, discloses a system and method for dynamically remapping at-risk memory areas in which when all copying has completed, the system management software programs the memory controller to target all memory accesses to the reserve SIMM, and the suspect SIMM is no longer used (col. 3, lines 38-42).

Jeddeloh and Vivio are analogous art in that they are of the same field of endeavor, that is, a system for the handling of memory errors in a computer system. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include this step because it would help to reserve areas of memory and maintain memory coherency (abstract), as taught by Vivio.

6. Claims 17-19, 21-28, 35-38 and 40-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh (US Patent No. 6,363,502) and Vivio et al (US Patent No. 5,867,642) and further in view of Nguyen et al (US PGPub No. 20040143719).

For claim 17, Jeddeloh discloses the invention as claimed above in the previous paragraphs. Jeddeloh does not, however, expressly disclose selectively

copying contents of a first memory location to a second memory location, logically replacing the first memory location with the second memory location, or initiating memory testing of the first memory location without an operating system interaction.

Vivio, however, discloses:

selectively copying contents of a first memory location to a second memory location (the system management software also proceeds to copy memory from the suspect SIMM to the reserve SIMM, col. 3, lines 29-30); and

logically replacing the first memory location with the second memory location (when all copying has completed, the system management software programs the memory controller to target all memory accesses, reads and writes, to the reserve SIMM, and the suspect SIMM is no longer used, col. 3, lines 38-42).

Despite these teachings, Vivio does not expressly disclose initiating memory testing of the first memory location without an operating system interaction.

Nguyen, however, discloses a computer system that may operate a portion of available memory as backup to a primary memory (abstract), mapping this memory portion to another region and then allow the memory testing program to perform a memory test (par. 0028 and fig. 3, items 76-78). Furthermore, Nguyen discloses that this memory testing may be performed in a system management mode, which allows testing of the memory without the help, or intervention, of the operating system, and thus is transparent to it (par. 0024).

Jeddeloh, Vivio and Nguyen are analogous art in that they are of the same field of endeavor, that is, a system and method for the remapping and backing up of memory that many contain data errors. It would have been obvious to a person of ordinary skill in the art at the time of the invention to allow such a system and method to operate without an operating system interaction because this would sustain operation in spite of hardware failures, which would be important in a mission-critical system (par. 0001). Further, the inability to check for memory errors in an operational computer system may lead to failures in unexpected situations such as a computer system crash (par. 0003 and par. 0005), as taught by Nguyen.

Claim 18 is rejected using the same rationale as for the rejection of claim 17 above. Nguyen further discloses access to the contents of the first memory location as copied to the second memory location can continue concurrently with the memory testing (memory testing procedures may be performed after POST procedures have complete, and during run-time of the computer system, par. 0025).

Claim 19 is rejected using the same rationale as for the rejection of claim 17 above. Vivio further discloses memory testing of the first memory location can continue without consuming a non-memory operating system resource (dynamically remapping memory from an at risk memory area, to a reserve memory area while maintaining memory coherency, and without affecting system operation or denying other applications or devices from accessing memory for an extended period of time, col. 7, lines 66-67 and col. 8, lines 1-4).

Claim 21 is rejected using the same rationale as for the rejection of claim 5 above. Vivio further discloses the first memory location is logically replaced by the second memory location by reconfiguring address resolving means (reads are targeted to the initial SIMM until all blocks have been copied, and that when all copying has completed, the system management software programs the memory controller to target all memory accesses, reads and writes, to the reserve SIMM, and the suspect SIMM is no longer used. col. 3, lines 38-42).

Claim 22 is rejected using the same rationales as for the rejections of claims 5 and 17 above.

Claim 23 is rejected using the same rationales as for the rejections of claims 5 and 17 above.

For claim 24, Jeddeloh discloses providing a report concerning a quality of the first memory location, where the quality data is based, at least in part, on the testing of the first memory location (a processor that determines whether an error correction code, known as the syndrome, indicates that there is an error in the memory portion that was read, col. 7, lines 24-26).

Claim 25 is rejected using the same rationale as for the rejection of claim 24 above. Jeddeloh further discloses storing a quality data associated with the quality of the first memory location, where the quality data is based, at least in part, on the testing of the first memory location (the error correction module writes the modified data word and syndrome to the requested memory bank, col. 7, lines 14-16).

Claim 26 is rejected using the same rationale as for the rejection of claim 17 above. Ngueyn further discloses testing the first memory location includes two or more test methods (if the computer system is relatively lightly loaded, it may be possible to perform detailed memory error testing procedures, such as walking zeros and/or walking ones in each memory location, par. 0025).

Claim 27 is rejected using the same rationale as for the rejection of claim 17 above. Nguyen further discloses the first memory location can be tested by one or more of, a parity test, an electrical test, a striping test, a marching one test, a marching zero test, and a pattern test (it may be possible to perform detailed memory error testing procedures, such as walking zeros and/or walking ones in each memory location, par. 0025).

Claim 28 is rejected using the same rationale as for the rejection of claim 21 above.

Claim 35 is rejected using the same rationale as for the rejection of claim 17 above.

Claim 36 is rejected using the same rationale as for the rejection of claim 21 above.

Claim 37 is rejected using the same rationales as for the rejection of claims 5 and 17 above.

Claim 38 is rejected using the same rationale as for the rejection of claim 17 above. Nguyen further discloses steps involving an operating system transparent system for on-the-fly memory testing:

a memory location identifying logic configured to identify a target memory location and a replacement memory location (par. 0028, fig. 1 and fig. 3);

a programmable memory address resolving logic configured to provide access to the target memory location and the replacement memory location (par. 0028, fig. 1 and fig. 3); and

a test controlling logic operably connected to the programmable memory address resolving logic, the test controlling logic configured to selectively program the programmable memory address resolving logic to divert memory accesses from the target memory location to the replacement memory location and to initiate testing of the target memory location (par. 0028, fig. 1 and fig. 3),

where the memory location identifying logic, the programmable memory address resolving logic, and the test controlling logic do not consume operating system resources (par. 0024).

Claim 40 is rejected using the same rationales as for the rejections of claims 2 and 38.

Claim 41 is rejected using the same rationale as for the rejection of claim 5 above. Vivio further discloses the test controlling logic is also configured to selectively reprogram the programmable memory address resolving logic to stop diverting memory accesses from the target memory location to the replacement memory location (when copying is completed, accesses are remapped to the reserve memory area, and normal operation is resumed, col. 7, lines 57-59; when an at risk SIMM is detected and the dynamic memory remapping to the reserve SIMM is completed, the system management controller will generate a

warning message to the computer system user indicating which SIMM is the at risk SIMM so that it may be replaced, col. 7, lines 34-39).

Claim 42 is rejected using the same rationale as for the rejection of claims 5 and 17 above.

Claim 43 is rejected using the same rationale as for the rejection of claims 5 and 17 above.

Claim 44 is rejected using the same rationale as for the rejection of claim 38 above.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh (US Patent No. 6,363,502) and Chauvel et al (US PGPub No. 20040024970).

For claim 4, Jeddeloh discloses the invention as per the rejection of claim 1 above. Jeddeloh does not, however, expressly disclose the memory quality assurance logic is configured to select the first memory location by one or more of, a linear method, a round-robin method, a random method, a least frequently used method, a most frequently used method, a most recently exhibiting an error method, and a least recently exhibiting an error method.

Chauvel, however, discloses a method for managing memory in which replacement algorithms may include, random replacement, round robin replacement, and least recently used replacement (par. 0018).
Jeddeloh and Chauvel are analogous art in that they are of the same field of endeavor, that is, a method for memory management. It would have been

obvious to a person of ordinary skill in the art at the time of the invention to include such methods for managing memories because this may reduce the number of memory accesses and overall power consumption (abstract), as taught by Chauvel.

8. Claims 20 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh (US Patent No. 6,363,502), Vivio et al (US Patent No. 5,867,642), Nguyen et al (US PGPub No. 20040143719), and in further view of Chauvel et al (US PGPub No. 20040024970).

Claim 20 is rejected using the same rationale as for the rejection of claims 4 and 17 above.

Claim 39 is rejected using the same rationale as for the rejection of claims 4 and 38 above.

9. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh (US Patent No. 6,363,502) and Mellor et al (US PGPub No. 20040169885).

For claim 31, Jeddeloh discloses the invention as per the rejection of claim 29 above. Jeddeloh does not, however, expressly disclose the system is embedded in an image forming device.

Mellor, however, discloses a method embodiment for memory management in which print job data is stored in the memory of an image forming device (abstract).

Jeddeloh and Mellor are analogous art in that they are of the same field of endeavor, that is, a method embodiment for memory management. It would have been obvious for a person of ordinary skill in the art at the time of the invention to include such an image forming device because this allows the processing of a print job and producing of an image such as text and/or graphics on a media sheet (par. 0020) as taught by Mellor.

Contact Information

10. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 8:30am-5pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan, is also reachable at 571-272-4210.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

10-31-05

DK

PIERRE VITAL
PRIMARY EXAMINER